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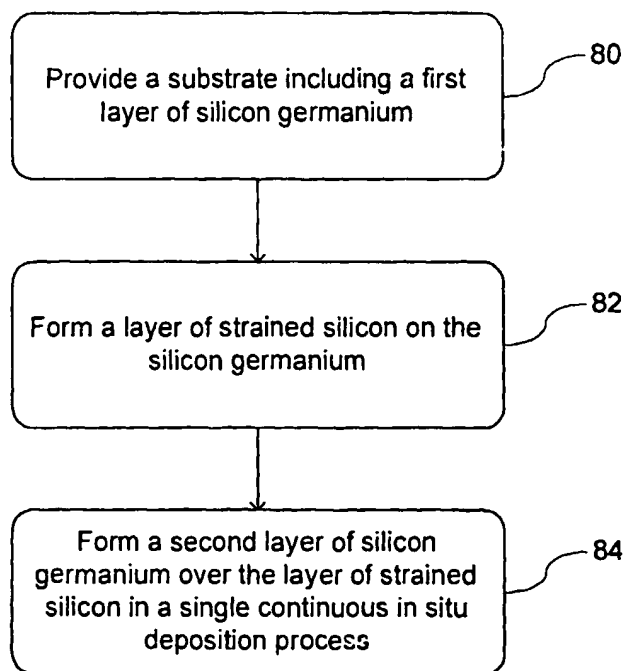
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(54) Title: METHOD OF FORMING A THICK STRAINED SILICON LAYER AND SEMICONDUCTOR STRUCTURES INCORPORATING A THICK STRAINED SILICON LAYER



(57) Abstract: A strained silicon layer (50) is grown on a layer of silicon germanium (40) and a layer of silicon germanium (52) is grown on the strained silicon (50) in a single continuous in situ deposition process with the strained silicon (50). Shallow trench isolations (48) are formed in the lower layer of silicon germanium (40) prior to formation of the strained silicon layer (50). The two silicon germanium layers (40, 52) effectively provide dual substrates at both surfaces of the strained silicon layer (50) that serve to maintain the tensile strain of the strained silicon layer (50) and resist the formation of misfit dislocations that might otherwise result from temperature changes during processing. Consequently the critical thickness of strained silicon (50) that can be grown without significant misfit dislocations during later processing is effectively doubled for a given germanium content of the silicon germanium layers (40, 52). The formation of shallow trench isolations (48) prior to formation of the strained silicon layer (50) avoids subjecting the strained silicon (50) layer to extreme thermal stresses and further reduces the formation of misfit dislocations.



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# INTERNATIONAL SEARCH REPORT

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## A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L21/20

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/104993 A1 (FITZGERALD EUGENE A ET AL) 8 August 2002 (2002-08-08) paragraph '0012!; figure 1b	1,2,8
X	WO 02/103760 A (AMBERWARE SYSTEMS CORP) 27 December 2002 (2002-12-27) figure 8	1,2,4,6, 8,10 7
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☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	COLLAERT N ET AL: "HIGH-PERFORMANCE STRAINED SI/SIGE PMOS DEVICES WITH MULTIPLE QUANTUM WELLS" 2002 IEEE SILICON NANOELECTRONICS WORKSHOP, vol. 1, no. 4, 9 June 2002 (2002-06-09), pages 190-194, XP001186516 HONOLULU ISSN: 1536-125X page 190, right-hand column, paragraph 3; figure 1	1,2,4,8
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Information on patent family members

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